- Qualified for Automotive Applications
- A

The SCT61450S device is a wide input power management IC with five channels output. The device is designed for So

- One Synchronous LV Boost Converter VOUT4:
  - Up to 500mA Continuous Output Current
  - Output Voltage of 5V
- One Load Switch VOUT5:
  - Up to 800mA Continuous Output Current

Programmable Power Sequencer for VOUT2, VOUT3, VOUT4 and VOUT5

- RESETB Output for System Management
- Simple/QA Watchdog
- Integrated Protection Features:
  - Hiccup Over Current Protection
  - Output Over-voltage/Under-voltage Protection
  - Adjustable Input Voltage Under-Voltage Lockout
  - Thermal Shutdown Protection
- Functional Safety Features:
  - Compliance with ISO26262 Development
  - Hardware Integrity up to Support ASIL-B System
  - ASIL-B Device Certification by TUV
  - BIST
- Up to 1MHz I2C Interface with Optional Packet Error-Checking (PEC)

- Available in QFN-24 (4mm*4mm)

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NAME	NO.	DESCRIPTION

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Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT2}	LV buck2 output voltage range	0.8	2.35	V
V_{OUT3}	LV buck3 output voltage range	0.8	2.35	V
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

PARAMETER	THERMAL METRIC	QFN-24	UNIT
R - $	Junction to ambient thermal resistance(1)	39.68	°C/W
JT	Junction-to-top characterization parameter	1.78	
JB	Junction-to-board characterization parameter(1)	3.26	
R - & W R S	Junction to case (top) thermal resistance(1)	24.67	
R - %	Junction to board thermal resistance(1)	3.46	

(1) SCT provides R - $ and R - & numbers only as reference to estimate junction temperatures of the devices. R - $ and R - & are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61450S is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61450S. Changing the design or9 0 Td [(C)3d ( )Tj -4cs sucTj 0[(gn or)2 6j 0 Tc 3f(

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage					
$V_{IN\_UVLO\_RISING}$	Input UVLO rising threshold	VIN_START[1:0]=00b				
		VIN_START[1:0]=01b				
		VIN_START[1:0]=10b				
		VIN_START[1:0]=11b	5.8	6	6.2	V
$V_{IN\_UVLO\_FALLING}$	Input UVLO falling threshold	VIN_STOP				

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VOUT1 (HV Buck)						
V_{ACC1}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%
R_{DSON_H1}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		75	150	P Ÿ
R_{DSON_L1}	Low-side MOSFET on-resistance			50	120	P Ÿ
I_{LIM_HS1}	High-side power MOSFET current limit		4.2	5.2	6.2	A
I_{LIM_LSP1}	Low-side power MOSFET positive current limit		3.2	4.2	5.2	A
I_{LIM_LSN1}	Low-side power MOSFET negative current limit		0.8	2	3.2	A
R_{DIS1}	Discharge resistance	Output disabled		100	200	Ÿ
t_{ON_MIN1}	Minimum on-time			80		ns
$_{Phase1}$(1)	Switching phase			0		deg
VOUT2 (LV Buck)						
V_{S2}(1)	Supply voltage range		3		5.5	V
V_{ACC2}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%
R_{DSON_H2}	High-side MOSFET on-resistance			65	150	P Ÿ
R_{DSON_L2}	Low-side MOSFET on-resistance			50	120	P Ÿ
I_{LIM_HS2}	High-side power MOSFET current limit		2.8	3.6	4.4	A
I_{LIM_LSP2}	Low-side power MOSFET positive current limit		2.2	3.2	4.2	A
I_{LIM_LSN2}	Low-side power MOSFET negative current limit		1	2	3	A
R_{DIS2}	Discharge resistance	Output disabled		50	100	Ÿ
t_{ON_MIN2}	Minimum on-time			90		ns
$_{Phase2}$(1)	Switching phase			0		deg
VOUT3 (LV Buck)						
V_{S3}(1)	Supply voltage range		3		5.5	V
V_{ACC3}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%
R_{DSON_H3}	High-side MOSFET on-resistance			65	150	P Ÿ
R_{DSON_L3}	Low-side MOSFET on-resistance			50	120	P Ÿ
I_{LIM_HS3}	High-side power MOSFET current limit		2.8	3.6	4.4	A

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Switching Frequency						
F_{SW}	LV Buck&Boost Switching frequency		1.98	2.2	2.42	MHz

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

I2C Interface

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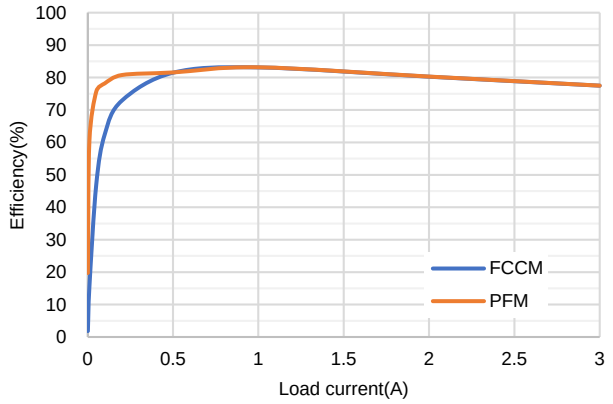
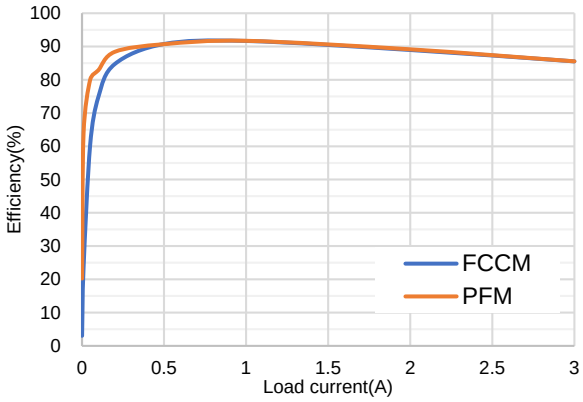
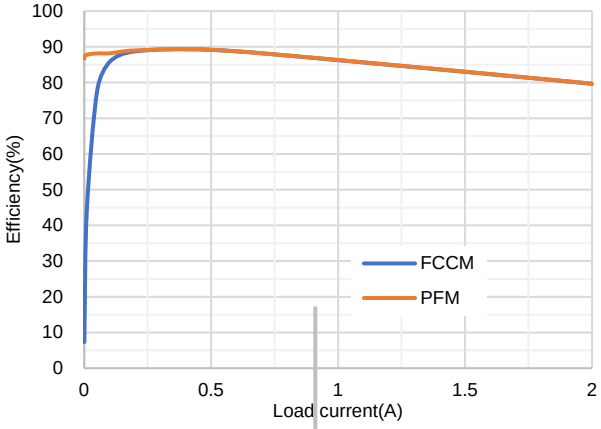
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



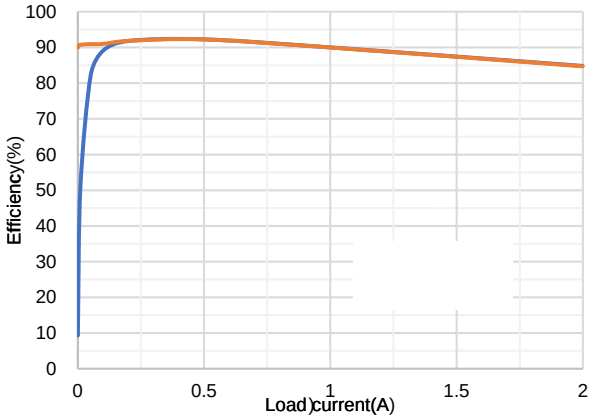
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=2.2MHz



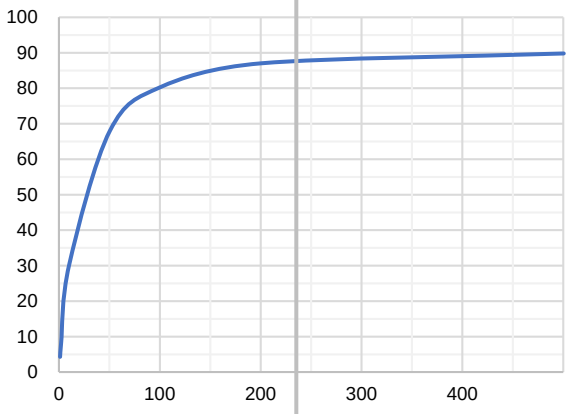
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=400kHz



Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V



Buck2 3 Efficiency vs Load Current, $V_{OUT2/3}$=1.8V



Boost Efficiency vs Load Current, V_{OUT4}=5V

(%)

Shutdown Current vs Temperature

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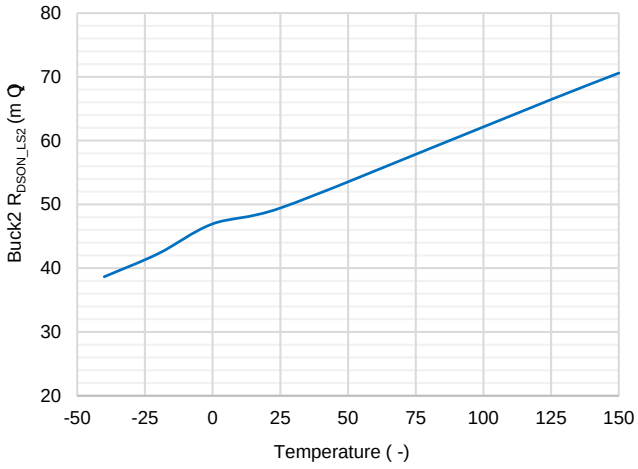
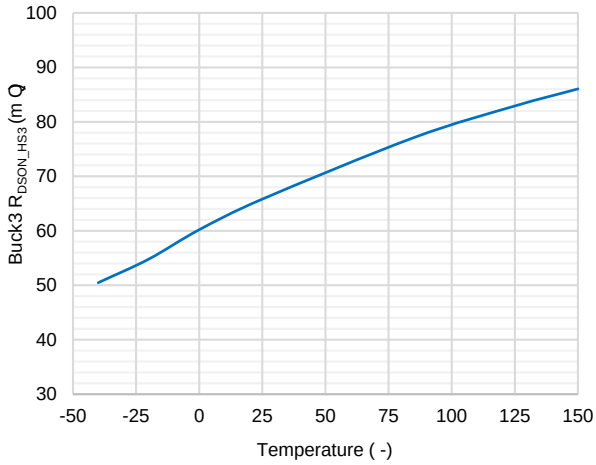
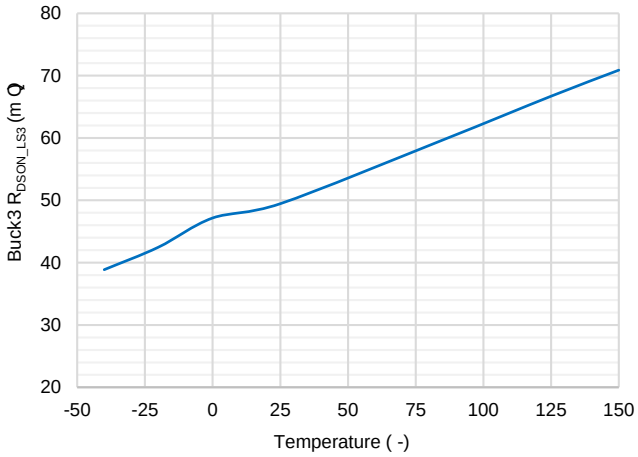
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



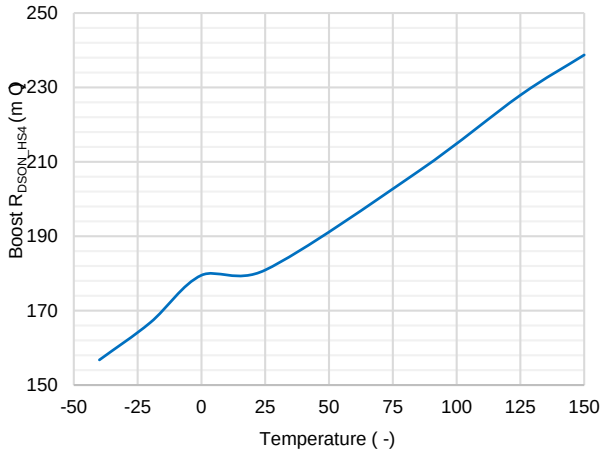
Buck2 R_{DSON_LS2} vs Temperature



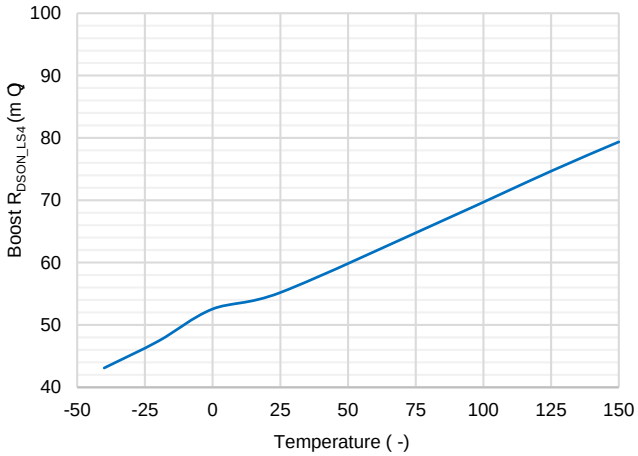
Buck3 R_{DSON_HS3} vs Temperature



Buck3 R_{DSON_LS3} vs Temperature



Boost R_{DSON_HS4} vs Temperature



Boost R_{DSON_LS4} vs Temperature

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Overview

The SCT61450S device is a wide input power management IC with five channels output. The device is designed for SoCs in automotive and industrial radar applications. The SCT61450S integrates one 3A HV Buck, two identical 2A LV Bucks, one 500mA LV Boost and one 800mA LV Load Switch. Each channel output is continuously monitored, any over-voltage/under-voltage fault will trigger RESETB pull low. Any deep over-voltage/under-voltage will be detected and the device will enter DEEPSAFE state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61450S device has protection features such as thermal shutdown, short-circuit protection and over-voltage/under-voltage protection. Sleep mode reduces the total supply current to 1 mA.

The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked before power up stage. Safety features ensure compliance with ISO26262 standard and functional safety up to ASIL-B level.

Operating State Machine

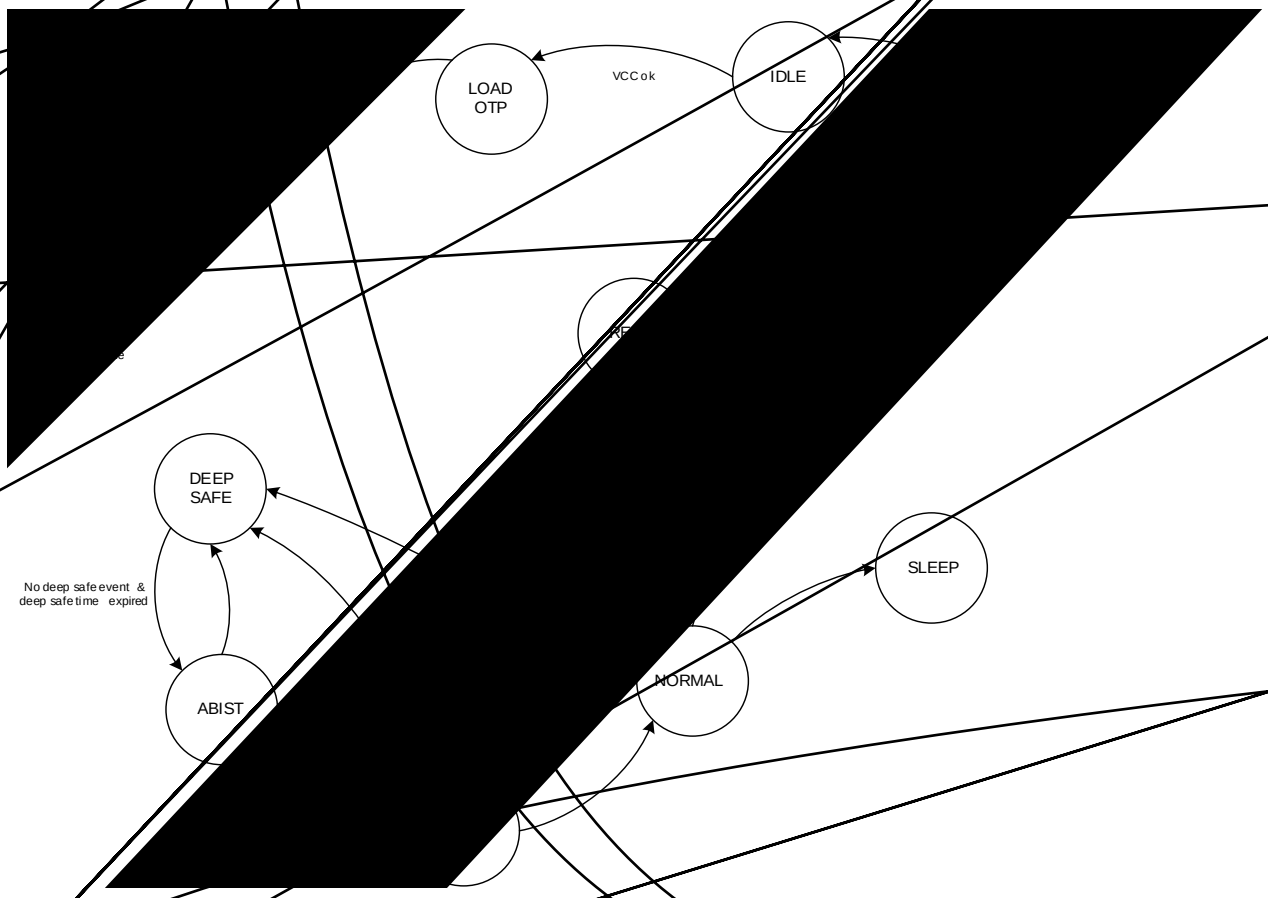

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Table 1. Sate and Function Matrix Table

State	Function											
	I2C	OTP load	Register reset	HV BUCK1	LV BUCK2	LV BUCK3	LV BOOST4	LOAD SWITCH5	Watchdog	OCP	DOVP/DUVP detect	TSD
IDLE	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LOADOTP	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LBIST	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DEEPSAFE	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
ABIST	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF			

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- VOUT5's output is out of deep OV/UV protection range or OCP
- Tj reaches Thermal Shutdown Point
- VIN/EN UVLO
- VCC OVP
- VIN OVP
- RESETB Stuck
- Loss of ground

ABIST State

To ensure safety mechanism work well, the device will check through all critical analog comparators before output start-up. If ABIST check is failed, the device will go back to DEEPSAFE state. ABIST will be implemented every time SCT61450S enter ABIST state, the device will transit to POWERUP state once ABIST is passed. Any ABIST failure will be recorded in register **SYS_STATE**.

POWERUP State

In POWERUP state, all rails will start-up following a dedicated sequence. Since the HV buck VOUT1 is the power supply for the other channels, VOUT1 is always set to start-up first. Then the other channels will rise after turn on delay time respectively. The turn on delay time for each is independent and can be adjusted via changing register **CONFIG_PU1** and **CONFIG_PU2**, thus flexible sequence is available. Deep OV/UV protection is activated to protect channels from destructive OV/UV risk. If all channels finish soft-start and they are within power good range, the RESETB rising timer begins. Once the timer is expired, the device will enter NORMAL state

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rail on, other rails are optional depending on register **CONFIG_ENLP**. Most unnecessary circuits will turn off to save power consumption. Deep safe event is still valid to provide protection. Note the RESETB pin is still high during this state to keep MCU alive. Once SLEEPB pin is pulled high longer than deglitch time, the device will exit from sleep mode and go to RECOVER state. The rest channels will then recover.

RECOVER State

Once the device is awake from sleep mode, the RECOVER state is an intermediate state before device go back to NORMAL state. The channels which are disabled in SLEEP state will start up according to programmed turn on delay. After all output are built up successfully, the device will then enter NORMAL state. If there is reset event during RECOVER state, the device will go to RCVRST state.

RCVRST State

RCVRST state is extra reset state to assert RESETB pin, other rails will still start up in programmed sequence. This state aims to provide possible reset events including OV/UV and watchdog detection for those continuously enabled rails. The device will go back to RECOVER state automatically after once the holding time is expired and no reset event.

VIN and EN UVLO

When the VIN pin voltage rises above 3.2V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 2.8V or when the EN pin voltage is below 1.0V.

EN pin is connected internally to ground allows the device to be disabled when EN pin is floating to simplify the system design.

High Efficiency Regulators

The switching frequency of HV Buck is 2.2MHz/400kHz selectable. All the LV bucks and one boost employ 2.2MHz fixed frequency peak current mode control. Forced continuous conduction mode (FCCM) allows the device to have a high output performance when light load. Built-in UVLO ensures all channels are capable of regulated output under the operating VIN range. Soft-start is fixed at 1ms for all channels. VOUT1 will always be the firstly built rail after power on, the other rails can be configured with range 0ms to 75ms turn on delay. Then the device can achieve a variety of sequence to fit power system.

The VOUT1 is a HV synchronous buck converter directly power from VIN pin. It's regulated at 3.3V with up to 3A continuous current. An external 100nF ceramic bootstrap capacitor between BST and SW1 pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. Note VOUT1 is the power supply for VOUT2/3/4/5.

The VOUT2 and VOUT3 are two identical LV synchronous buck converter power by VOUT1. Their output can be configured via I2C range from 0.8V to 2.35V with 50mV step. Each is capable of 2A continuous current. To further improve the EMI performance, the VOUT2 and VOUT3 will operate with 180 phase-shifted clock.

The VOUT4 is a LV synchronous boost converter also power by VOUT1. It's regulated at 5V with up to 500mA continuous current.

The VOUT5 is a load switch output powered by VOUT1, the integrated MOSFET on-resistance is 100 P

The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

Each output voltage is continuously monitored during operation, the OV/UV threshold can be adjusted independently in register **CONFIG_PGSEL1** and **CONFIG_PGSEL2**.

Deep Over Voltage Protection

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If any output exceeds the deep over voltage protection threshold 115%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_OVP_SEL[1:0]**.

Deep Under Voltage Protection

If an output falls below the deep under voltage protection threshold 75%, all outputs will shut off fo (out)3.5 et

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Sleep Mode

The SCT61450S integrates an ultra power-saving mode with VOUT1 on. When in sleep mode, the disabled channels will shutoff and the alive channels will operate under PFM to further improve efficiency. Only after all disabled channels shutoff, pulling SLEEPB pin high can wake up the device and exit sleep mode. It can coordinate with MCU to achieve sleep mode system with extremely low consuming current from battery. If **LOWPOWER_EN[0]**=0, the device will ignore the inputs from SLEEPB pin and never enter sleep mode.

There are two cases for the device to enter sleep mode: a) **LOWPOWER_EN[0]**=0 in OTP setting, the MCU must set bit **LOWPOWER_EN[0]**=1 in register **CONFIG_ENLP** to enable sleep mode first, then pull SLEEPB pin low. When the device exit sleep mode, the bit **LOWPOWER_EN[0]** will be reset automatically. b) **LOWPOWER_EN[0]**=1 in OTP setting, pull SLEEPB pin low will bring device to sleep mode directly. .024 0 o.5 (n l)1[(s)]T

LOWPOWER_EN[0]=10t10tr0si ((0)7.5m(i)1.7 ((he)0.6ag(e

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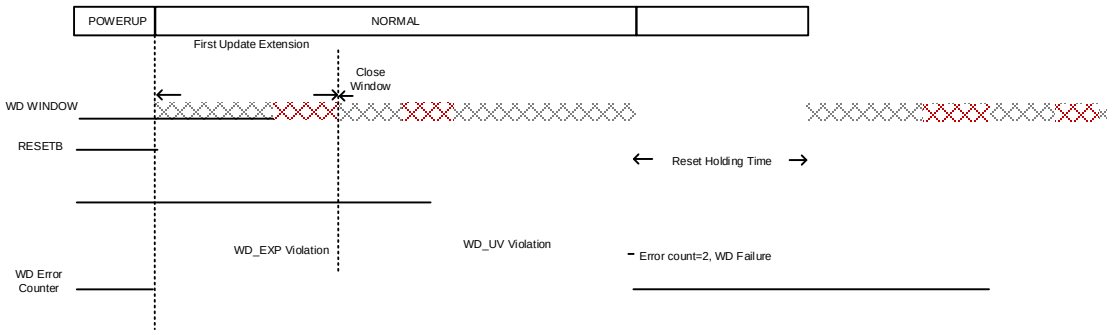

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I2C Interface

The SCT61450S integrates a two-wire serial interface for bidirectional communications between the device and the master through bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61450S is always assigned a unique chip address and operates as a slaver, the master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and SDA lines need a pull-up resistor connected to bus voltage since HIGH state is the default state when bus is idle. The SCT61450S supports Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of interfaces is limited.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

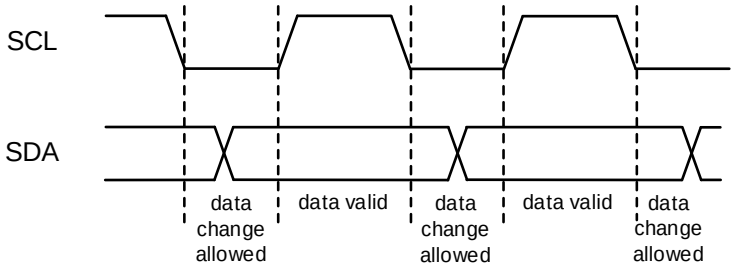

Figure 4. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Both the START and STOP conditions are generated by master on bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

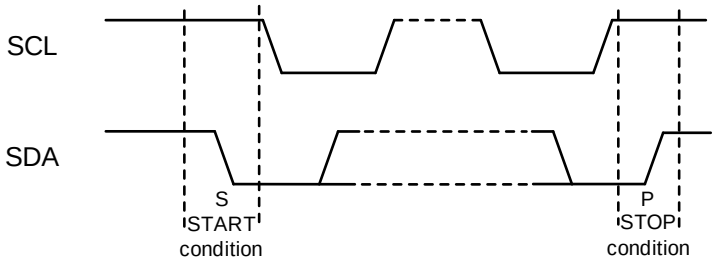

Figure 5. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61450S will pull the SDA line LOW during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled LOW. It's called not acknowledge signal and indicates the end opul0.7 (n)1.4M ( )0Dk1idn.

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indicate write command, and a 1 indicates read command. The slave address is factory-programmed between 0x38 through 0x3B, see DEVICE ORDER INFORMATION for details.

Packet Error Checking (PEC)

The SCTSsrslaetrgrg (rEtedu(r)-1.3 (i)1.4 (a)6.1 g ethe(I)3.6 2CDm71.7 (m)1.6 undicatE(c)-2 (a)6.1 (a)6.1 e

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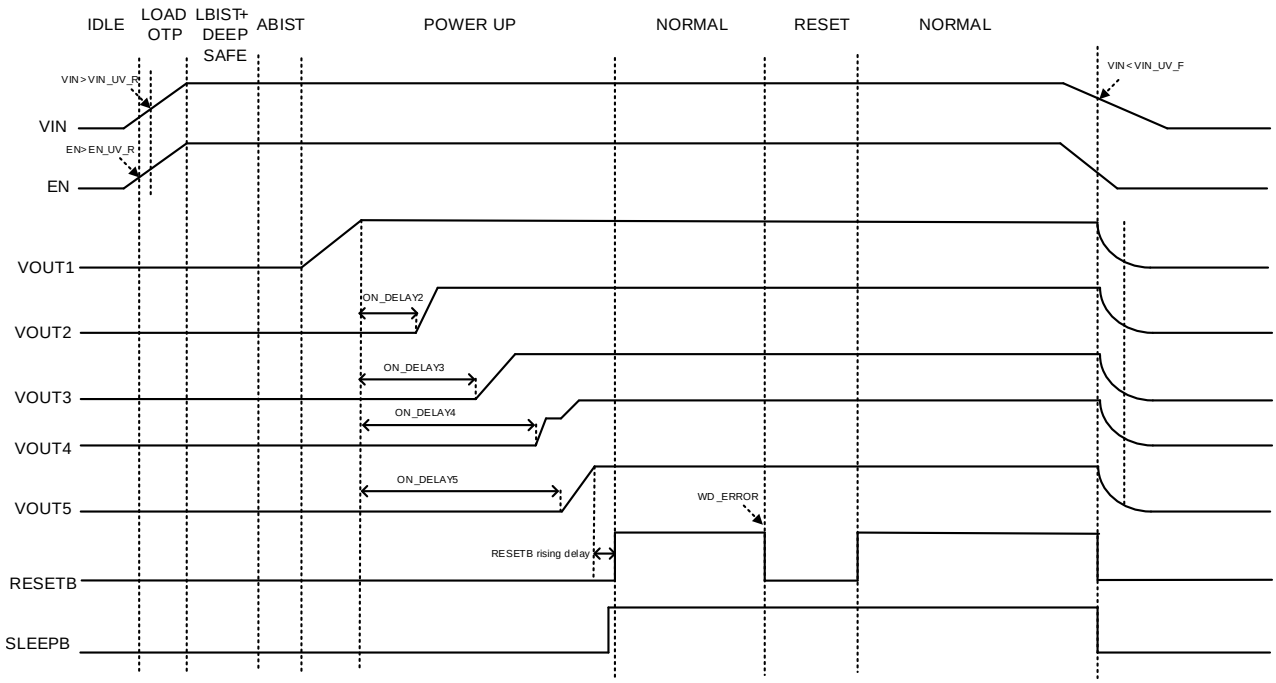
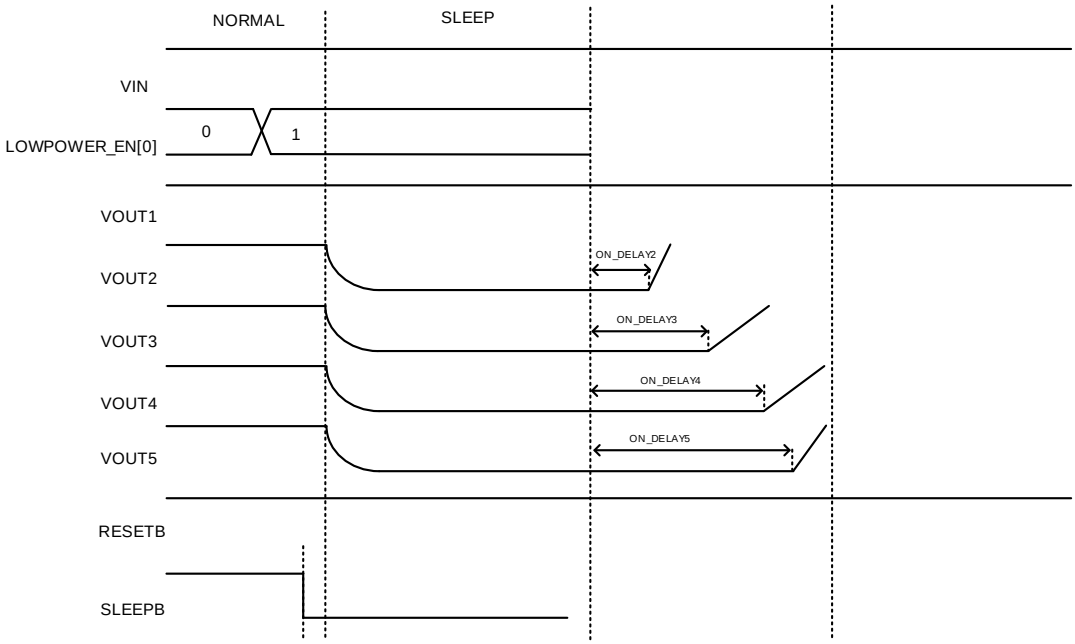


Figure 7. Power on Sequence



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Typical Application



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Under Voltage Lock-Out

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$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (10)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{RMS} = 0.5 \times I_{OUT} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 12 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For the boost converter power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 10) input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Bootstrap Capacitor Selection

$) F H U D P L F F D S D F L W R U P X V W S E H p l a c e d c l o s e t o t h e F W H G E H W Z H H Q %

For boost converter, typically, a 10) F ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. From the required output voltage ripple, use the below equation to calculate the minimum required effective capacitancec2(or uiL/P <</MCID10 >>BDC - 2(or u)-1.549-2.6 (c2(or uiEBT /P

Application Waveforms

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, V_{OUT5}=3.3V,unless otherwise noted

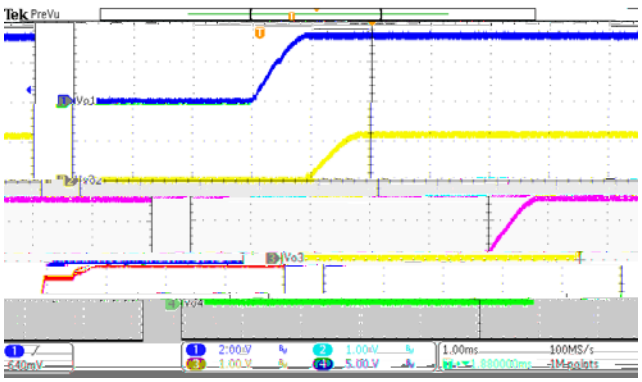

Figure 11. Power On (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)



Figure 12. Power On (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

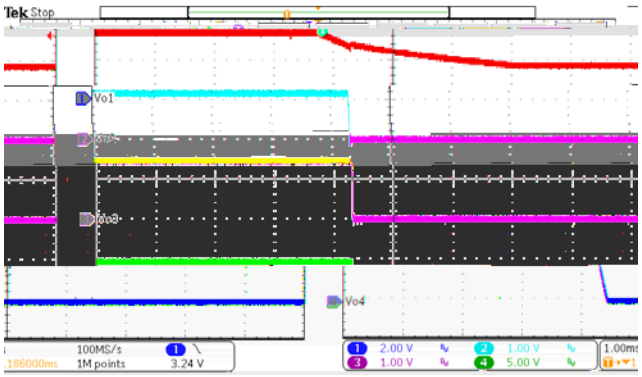

Figure 13. Power Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

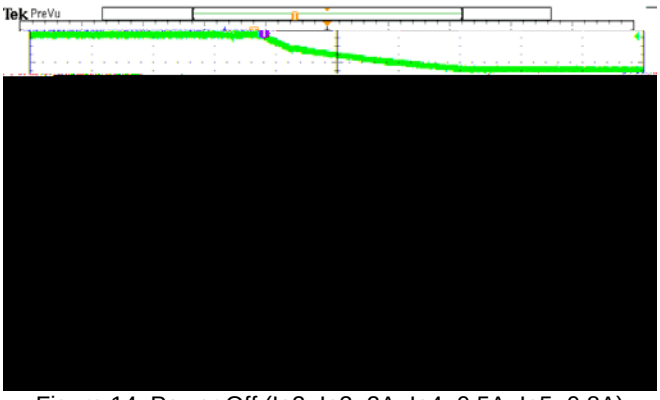

Figure 14. Power Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

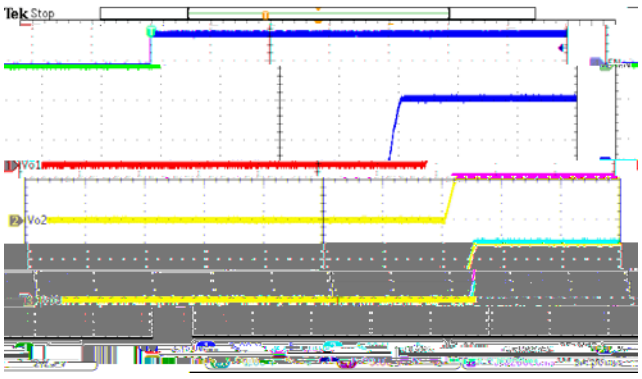

Figure 15. EN On (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

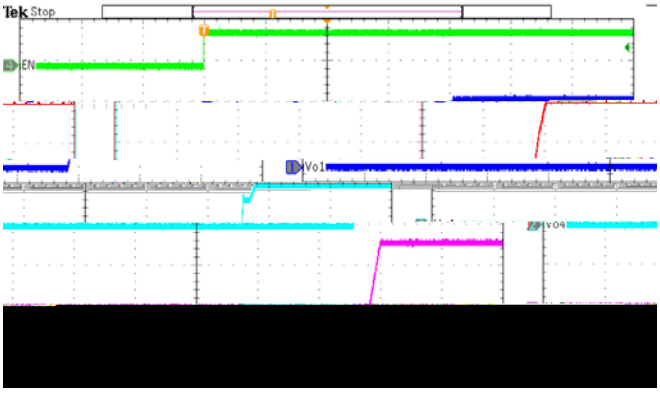

Figure 16. EN On (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

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Application Waveforms (continued)

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, V_{OUT5}=3.3V,unless otherwise noted

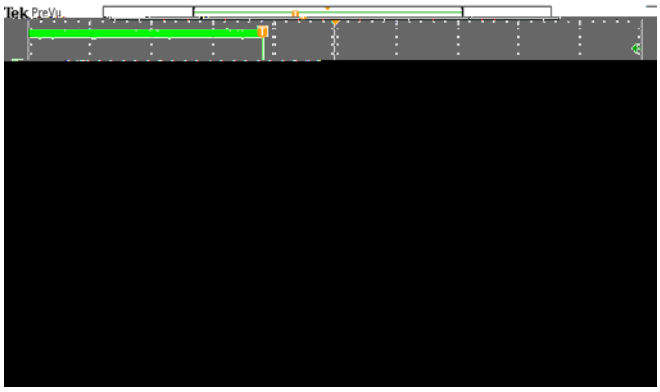

Figure 17. EN Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

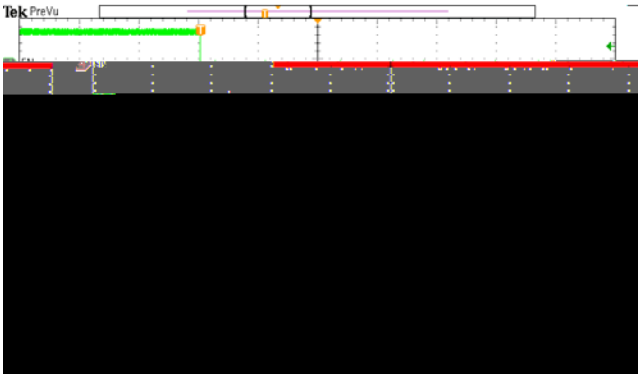

Figure 18. EN Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

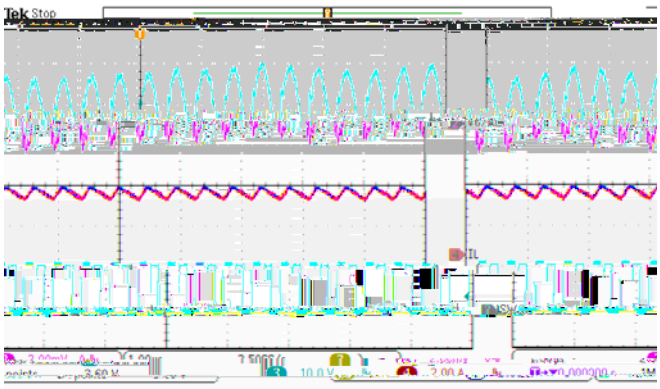

Figure19. Buck1 Steady State (Io1 = 3A)

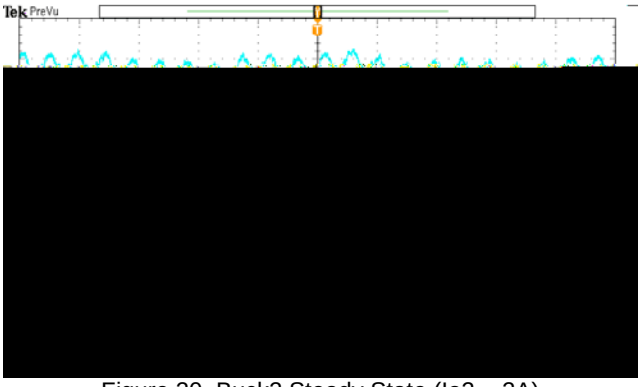

Figure 20. Buck2 Steady State (Io2 = 2A)

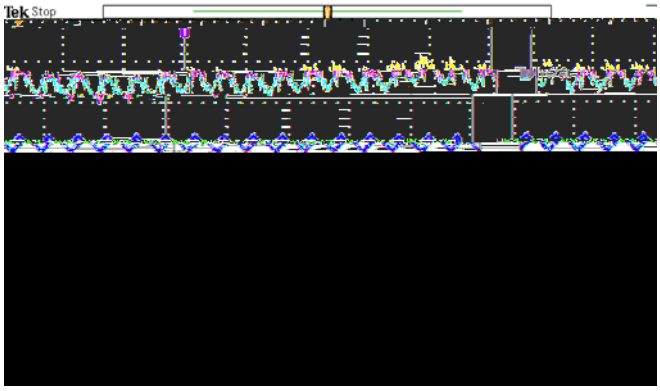

Figure 21. Buck3 Steady State (Io3 = 2A)

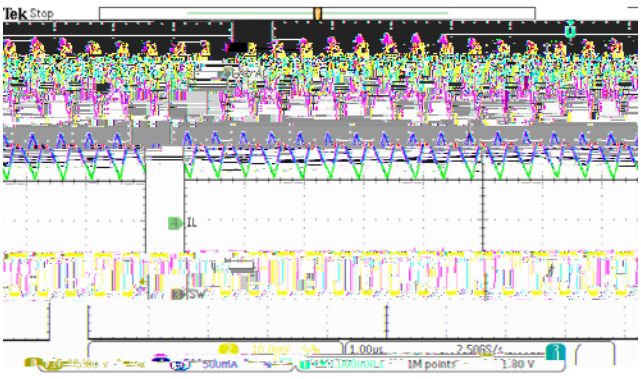

Figure 22. Boost4 Steady State (Io4 = 500mA)

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Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Make sure the ground path between VIN capacitor and PGND1 pin is shortest with low,ris sh(or)-1G (ond)6. (uen)6.1 (c)-

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Register Map

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C LOCK	WD LOCK
0x00	CHIPID	-	Y	N 2	re f

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CHIPID [7:0]				
ADDRESS: 0x00				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	Reserved

				11: Scale =5ms. Delay ranges from 0-75ms

CONFIG_T2 [7:0]				
ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	DF_SCALE	W/R	OV/UV Digital Filter. Adds additional filtering to all OV/UV comparators.	Analog Filter Time = 10µs. Added Digital Filter Timeo! =DF[4:0] x 2µs, when DF_SCALE=0, =DF[4:0] x 10µs, when DF_SCALE=1.
[4:0]	DF	W/R		

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STATUV [7:0]				
ADDRESS: 0x0A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	UV	Read Clear	UV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are above UV threshold after DF 1 = Any enabled channel is below UV threshold after DF
[6]	RESERVED	R	/	/
[5]	UV_WAR5	Read Clear	UV warning for OUT5, Digital Filter is not included	0 = OUT5 is above UV threshold before DF 1 = OUT5 is below UV threshold before DF

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[2]	OV_WAR2	Read Clear	OV warning for OUT2, Digital Filter is not included	0 = OUT2 is below OV threshold before DF 1 = OUT2 is above OV threshold before DF
[1]	OV_WAR1	Read Clear	OV warning for OUT1, Digital Filter is not included	0 = OUT1 is below OV threshold before DF 1 = OUT1 is above OV threshold before DF
[0]	RESERVED	R	/	/

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CONFIG_PFM [7:0]				
ADDRESS: 0x12				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RESERVED	R	/	/
[3]	PFM4	W/R	BOOST4 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[2]	PFM3	W/R	BUCK3 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[1]	PFM2	W/R		

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[2:0]	WD_1UD	W/R	First Update Extension. Sets the number of extra watchdog window cycles after POR to the normal watchdog window.

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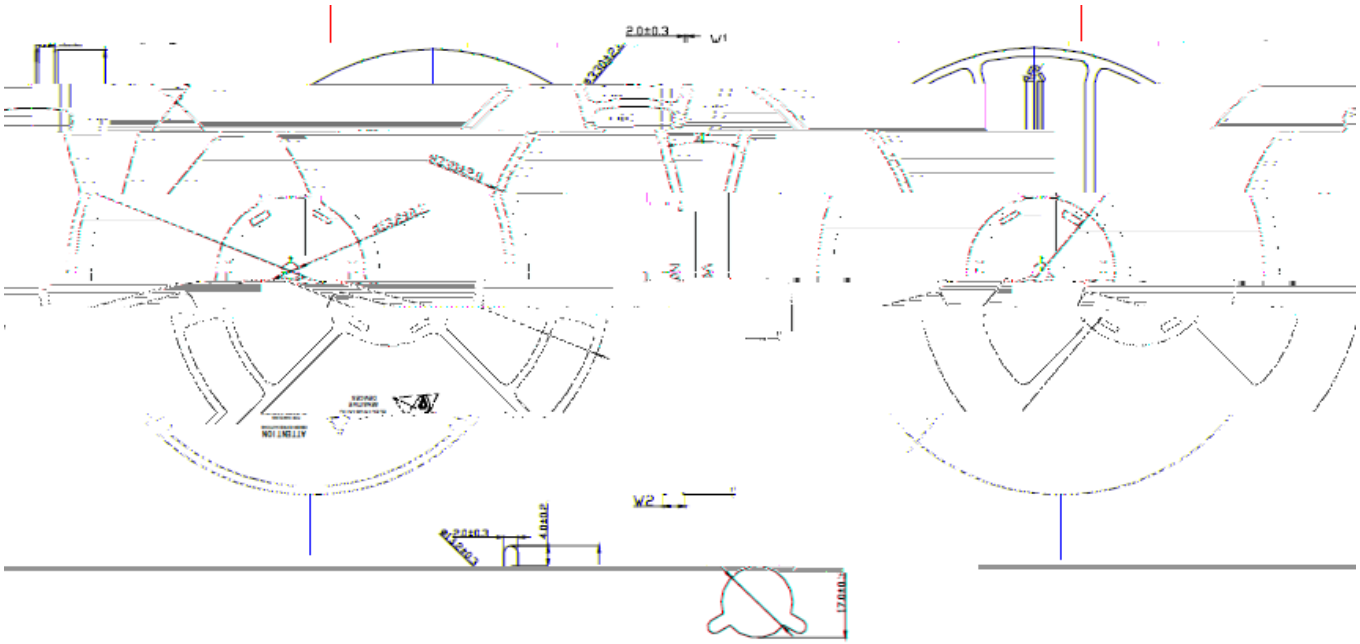



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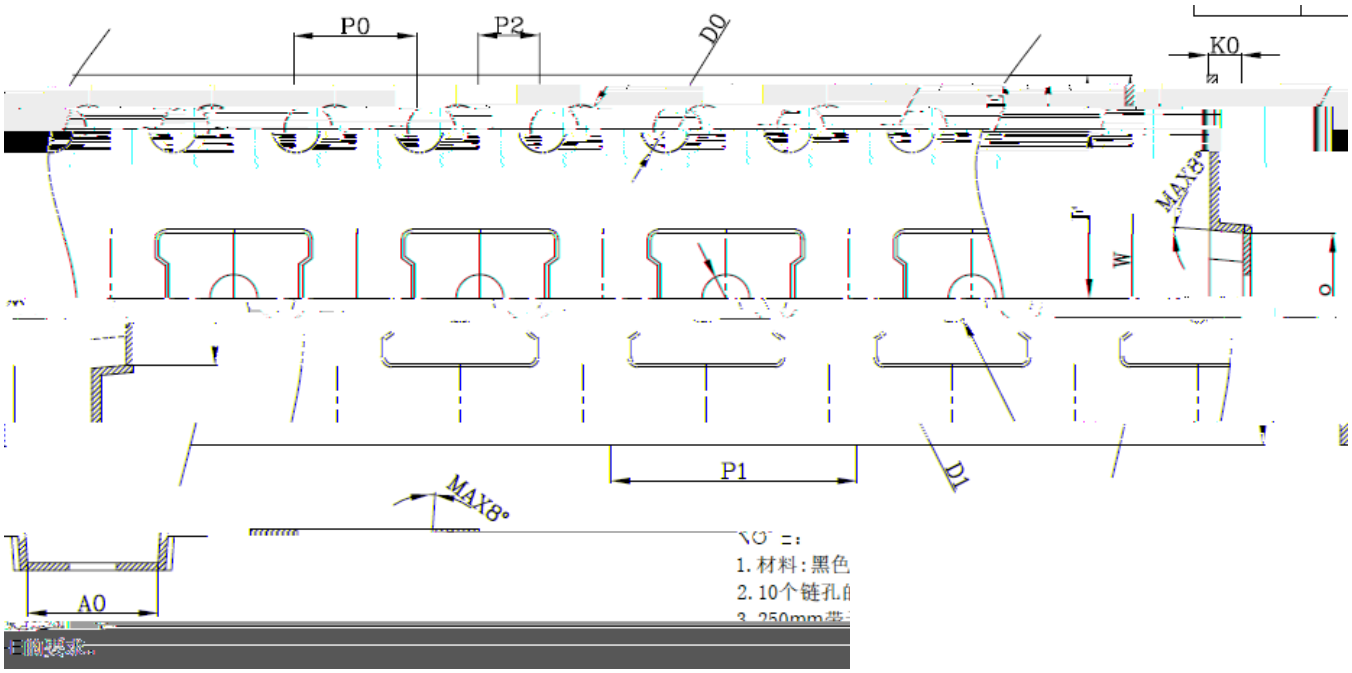

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	2.00±0.05	4.30±0.10	4.30±0.10	1.10±0.10	4.00±0.10	8.00±0.1

W	SYMBOL	T	E	F	D0	D1
SPEC		0.30±0.05	1.75±0.10	5.50±0.05	1.55±0.05	1.55±0.1

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